Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. An electro-magnetic interference protection circuit for a clock buffer, comprising:
a clock buffer, for receiving a clock signal and buffer-outputting said clock signal;
a ferrite bead, wherein said ferrite bead is connected in serial with a power source of said clock buffer to protect said clock buffer from electro-magnetic interference; and
a capacitor, wherein said capacitor is connected in parallel with said ferrite bead to reduce the distortion of said clock signal due to said ferrite bead.

[c2] 2. The electro-magnetic interference protection circuit for a clock buffer of claim 1, wherein an impedance of said ferrite bead is at a maximum at a frequency of said electro-magnetic interference.

[c3] 3. The electro-magnetic interference protection circuit for a clock buffer of claim 1, wherein a frequency of said electro-magnetic interference is 125MHz.

[c4] 4. The electro-magnetic interference protection circuit for a clock buffer of claim 1, wherein an impedance of

said capacitor is at a minimum at a frequency of said clock signal.

[c5] 5. The electro-magnetic interference protection circuit for a clock buffer of claim 1, wherein a frequency of said clock signal is 25MHz.

[c6] 6. An electro-magnetic interference protection method for a clock buffer, comprising the steps of: connecting a ferrite bead in serial with a power source of said clock buffer to protect said clock buffer from electro-magnetic interference; and connecting a capacitor in parallel with said ferrite bead to reduce the distortion of a clock signal outputting by said clock buffer due to said ferrite bead.

[c7] 7. The electro-magnetic interference protection method for a clock buffer of claim 6, wherein an impedance of said ferrite bead is at a maximum at a frequency of said electro-magnetic interference.

[c8] 8. The electro-magnetic interference protection method for a clock buffer of claim 6, wherein a frequency of said electro-magnetic interference is 125MHz.

[c9] 9. The electro-magnetic interference protection method for a clock buffer of claim 6, wherein an impedance of said capacitor is at a minimum at a

frequency of said clock signal.

[c10] 10.The electro-magnetic interference protection circuit for a clock buffer of claim 6, wherein a frequency of said clock signal is 25MHz.